Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application. No changes to the claims are made herein.

Listing of Claims:

1. **(Previously Amended)** A method for programming field programmable gate arrays (FPGA) operatively connected to a bus system of a computer device with configuration data, the method comprising by the steps of:

(a) using a device driver to read the configuration data from a storage device operatively connected to the bus system of said computer device;

(b) providing the configuration data to the FPGA by way of the bus system of said computer device;

(c) programming the configuration data into an electrical erasable programmable read only memory (EEPROM) connected with said FPGA via a multiplexer, hereinafter referred to as a MUX element, adapted such that the configuration data is capable of being read from the FPGA to the EEPROM;

(d) switching said MUX element such that the configuration data is capable of being read from said EEPROM into said FPGA; and

(e) programming the configuration data from the EEPROM to said FPGA.

2. **(Previously Amended)** A method for using field programmable gate arrays (FPGAs) and an electrical erasable programmable read only memory (EEPROM) connected to said FPGA via a multiplexer, hereinafter referred to as a MUX element, the method comprising the steps of:

(a) controlling said MUX element in order to be able to read a schema from said FPGA into said EEPROM;

(b) storing said schema in said EEPROM;

(c) controlling said MUX element in order to be able to read said schema from said EEPROM into said FPGA; and

(d) triggering a configuration of said FPGA by feeding a said schema from said EEPROM to said FPGA.

3. **(Previously Amended)** A hardware circuit arrangement having a programmable read only memory (PROM) device, an electrical erasable programmable read only memory (EEPROM) device, a field programmable grate array (FPGA) device accessible via a computer bus system and a multiplexer, hereinafter referred to as a MUX element, connected between said devices, said circuit arrangement comprising:

(a) said PROM device being arranged for comprising control data for proper recognition of said FPGA by said bus system, and a logic usable for programming said EEPROM device with an EEPROM-FPGA interface;

(b) said MUX element being controllable to permit data to be read from either said PROM device or said EEPROM device or said FPGA device, in order to properly connect said FPGA to said bus system and to initialize a configuration of said FPGA with contents comprised of said EEPROM.

4. **(Previously Amended)** The circuit arrangement according to claim 3, wherein the circuit arrangement is located on a PC-card detectable by a PC system bus.